REMARKS

The application was filed on 10 September 1999 with twenty-one claims. In the first Examiner's Office Action mailed 03 October 2002, the Examiner rejected claims 4-7, 17, 16 and 19 under 35 U.S.C. §112; the Examiner further rejected claims 19 and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,385,708 entitled, "Using a Timing-Look-Up-Table and Page Timers to Determine the time Between Two Consecutive Memory Accesses," to Stracovsky et al. (Stracovsky '708). The Examiner further rejected claims under 35 U.S.C. §103(a) as being unpatentable over Stracovsky '708 in view of U.S. Patent No. 6,088,772 entitled, "Method and Apparatus for Improving System Performance when Reordering Commands," to Harriman et al. (Harriman '772). Applicants revised the specification at the request of the Examiner and amended claims 1, 16, 17, and 19 to remove rejections under 35 U.S.C. §112. Applicants traversed the rejection of claims 19 and 20 under 35 U.S.C. §102(e) in light of Stracovsky '708 and of claims 1-21 under 35 U.S.C. §103(a) in view of Stracovsky '708 and Harriman '772. Applicants submitted formal drawings.

In a responsive Office Action, the Examiner finally rejected claims 19 and 20 under 35 U.S.C. §102(e) in light of Stracovsky '708 and of claims 1-18, 21 under 35 U.S.C. §103(a) in view of Stracovsky '708 and Harriman '772. In this response to the final rejection of the claims, Applicants amend the claims to put them in condition for allowance and/or in better condition for appeal. Applicants respectfully request the Examiner to enter the amendments and consider them in view of the remarks below.

The Rejection Under 35 U.S.C. § 102(e)

The Examiner rejected claims 19 and 20 under 35 U.S.C. §102(e) alleging that Stracovsky '708 anticipates the claimed invention. Applicants respectfully traverse the rejection because Stracovsky '708 does not disclose "a plurality of comparison logic circuits, **each of said plurality of comparison logic circuits associated with each of said plurality of command FIFO queues** to determine which memory commands of each of said command types have the least memory cycle performance penalty" as in independent claim 19.

The Examiner refers to Stracovsky '708 at Figure 10, elements 1020 and 1022 as showing command FIFO queues. Elements 1020 and 1022 are write buffer and a read buffer, respectively. Data is transferred from the reordering block 1018 into the write buffer 1020 and read buffer 1022. From the write buffer 1020 data is transmitted to the data interface 1012 and a data bus 914; there is no comparison logic circuit associated with the write buffer 1020. Data from the read buffer 1022 is transmitted to the system interface 1002 and onto the system bus 906; again there is no comparison logic circuit associated with the read buffer 1022. Because a claimed element is not taught, disclosed, or inherent within the teachings of Stracovsky '708, a rejection under 35 U.S.C. §102(e) is not appropriate. The Examiner alleges, however, that column 20, lines 12-30 of Stracovsky '708 shows that there are comparison logic circuit associated with each of the command FIFO queues. Applicants respectfully disagree with the Examiner's assertion. Column 20, lines 12-30 of Stracovsky '708 discuss data fields of data pertaining to a specific embodiment of a reordering circuit in a memory controller which data is then forwarded to the write and read buffers. At column 19, line 63 through column 21, line 30, Stracovsky '708 teaches a command queue 1502 having six command queue

elements 1602, each of which store a command. Note that one command is stored in each queue element, not one command type as applicants have claimed, but one command. Therein lies the distinction. Moreover, the comparison of the data fields occurs in each command, i.e., the comparison logic circuit is not unique to a particular command type, but rather to six commands, regardless of type. If the Examiner persists in maintaining the rejection, Applicants request the Examiner to point out with particularity where Stracovsky '708 teaches a FIFO queue, one for each command type, and then a comparison logic circuit for each FIFO queue. Thus, Applicants respectfully traverse the rejection of the claims as being anticipated under 35 U.S.C. §102(e) by Stracovsky '708 because Stracovsky '708 does not teach that each of said plurality of comparison logic circuits is associated with each of said plurality of command FIFO queues, each of which is associated with a particular command type, as in independent claim 19. Similarly, by its dependence, claim 20 is also allowable.

The Rejection Under 35 U.S.C. § 103(a)

The Examiner has finally rejected claims 1-18 and 21 as being obvious in view of Stracovsky '708 in view of Harriman '722. Stracovsky '708, as explained, proposes a memory controller having a circuit to avoid data transfer collision of memory commands to the same memory bank. Harriman '722 teaches a memory access controller in which memory commands to the same memory portion are first collected and then commands to the same memory portion are continued to execute until a count is reached. It would appear, that Stracovsky '708 and Harriman '722 should not be combined, and even if they were combined, they still would not teach the apparatus and method of categorizing commands into queues based on type of command, and then

reordering the commands using comparison logic associated with each queue. First, Stracovsky '708 does not teach a FIFO queue associated with a particular command type in its reordering logic; Stracovsky '708 teaches six queues, each associated with a command, not a command type. Harriman '722 also does not teach or suggest a command FIFO queue, each associated with a unique command type. While it is possible to envision how Harriman '722 might be combined with Stracovsky '708, the combination of references do not teach Applicants' claimed invention of categorizing commands into types, putting each type into its own FIFO queue, reordering the commands of a particular type in its respective queue based on memory latency, and then arbitrating the commands. Indeed, Harriman '722 teaches against Applicants claimed invention, because Applicants in the originally filed specification, at page 17, lines 1-20, that the memory penalty of accessing the same memory bank, referred to as the precharge penalty, is greater than the memory penalty accessing a different memory bank or card, the switching penalty. Thus, one of skill in the art would not be inclined to consider either Stracovskly '708 but especially, not Harriman '722 when comparing memory cycle penalties.

Conclusion

Applicants have amended the claims in an attempt to put them in condition for allowance and/or in better condition for appeal. Applicants respectfully maintain that Stracovsky '708 does not teach the concept of having a unique queue for each command type, and then a comparison logic circuit for each separate command queue, wherein the commands in a particular queue are all of the same type and the comparison logic circuit compares the memory penalty associated with the commands of the same type in its queue. Applicants respectfully traverse the rejection of obviousness based on

Stracovsky '708 and Harriman '722 as above because Stracovsky '708 does not teach the unique and respective correspondence between the command type, the queue, and the comparison logic circuit; and further because Harriman '722 teaches a method to access the same the memory bank and Applicants teach that accessing the same memory bank would impose the largest memory cycle penalty. Applicants respectfully request the Examiner to enter the amendments, reconsider the application in view the amendments and the remarks, and pass the application to issuance. The Examiner is further invited to telephone the Attorney listed below if he thinks it would expedite the prosecution and the issuance of the patent.

Applicants respectfully request the Examiner to acknowledge the submission and acceptance of formal drawings.

Respectfully submitted,
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